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**Integrated chip package structure using silicon substrate and method of  
manufacturing the same**

Appl. No. : 10/755,042 Confirmation No. 8665  
Applicant : Mou-Shiung Lin,  
Jin-Yuan Lee,  
Ching-Cheng Huang  
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Examiner : Fenty, Jesse A  
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Customer No. : 27765

Commissioner for Patents  
P.O. Box 1450  
Alexandria VA 22313-1450

**AMENDMENT**

5 Sir:

In response to the Final Office action mailed Jan. 4, 2007, please consider the remarks as follows:

Remarks/Arguments begin on page 2 of this paper.

OK to Enter  
for 04/02/07